substrate and locally restricted to specific areas of the integrated circuit.

10. (New) The integrated circuit of claim 9, wherein the insulating layer is locally restricted to the area of at least one of an integrated inductance, integrated resistor, integrated capacitor, integrated bonding pad, and conductive path.

11. (New) The integrated circuit of claim 10, wherein the integrated inductance comprises at least an upper metal plane for realizing a spiral, an insulating layer, a lower metal plane for providing a connection for an internal contact, an insulation layer, a field oxide layer, a channel stop layer, the buried local insulating layer and the semiconductor substrate.

Cont. B1

12. (New) An integrated circuit of reduced parasitic capacitive influences, comprising:

a semiconductor substrate; and

an insulating layer of a thickness of at least 5 μm thickness buried in the substrate and locally restricted to the area of at least one of an integrated inductance, integrated resistor, integrated capacitor, integrated bonding pad and conductive path, wherein the integrated inductance comprises at least an upper metal plane for realizing a spiral, an insulating layer, a lower metal plane for providing a connection for an internal contact, an insulation layer, a field oxide layer, a channel stop layer, the buried local insulating layer and the semiconductor substrate.

Remarks.

The objection raised against the specification has been sought to be avoided by the above amendment to pages 1 and 6. In order to show that "a priori" is a foreign language expression (of the kind sometimes used in learned

English texts and meaning "derived by reason from self-evident propositions"), Applicants have amended it to be shown in italic letters.

While Applicants wish to express their appreciation for the Examiner's finding of allowability of claims 4-8, and of claim 3 if rewritten in independent form, they cannot, with respect, agree the Examiner's rejection of claims 1 and 2 under 35 U.S.C. 102(e) on grounds of alleged anticipation by Xie, U.S. patent 5,736,749. For Xie does not, in his Figs. 2A-2D disclose "an integrated circuit of reduced parasitic capacitive influences provided with an insulating layer (115) buried in the semiconductor substrate (100)" and "being at least 5 μm thick (i.e. 200 μm) and is locally restricted to specific areas of the integrated circuit...".

Having carefully considered the Xie reference, Applicant have concluded that it teaches an integrated circuit with an inductance below which there is disposed a layer of porous silicon. An insulating layer is superposed on the layer of porous silicon.

Referring to layer 20 (in Fig. 1) or 115 (in Fig. 2c), the Examiner has alleged that they anticipate Applicants' circuit. However, in accordance with Applicant's claim 1, the insulating layer is of a thickness of at least 5 μm. However, as described at col. 3, line 52-53 and col. 4, lines 22-24, Xie, insulating layer is of a thickness of from 10 to 1,000 nm. The sole purpose of this insulating layer of Xie's is to seal the porous silicon.

The Examiner's statement that Xie's insulating layer is 200 μm thick appears to be incorrect. The porous silicon layer has been described as having a thickness of 200 μm (see col. 4, line 10-13); but porous silicon is no insulator. As far as Applicants know, porous silicon is a semiconductive material and would, therefore, be unsuitable for purposes of Applicants' invention.

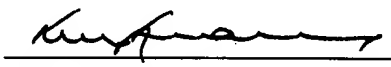
It is earnestly urged that current claims 1-2 define structure which is patentably distinct from Xie's invention and that they are allowable in their present form. Nevertheless, Applicants are submitting new claims 9-12. Claims 9-11 resemble claims 1-3; but are believed to worded more appropriately for

purposes of American patent practice. Claim 12 is claim 11 rewritten in independent form.

Copies of a substitute specification and claims incorporating the above amendment and the preliminary amendment of 20 June 2000 are enclosed in marked-up and clean versions; and it is hoped that these satisfy the present requirements governing amendments.

It is respectfully urged that as hereby amended, Applicants' instant application is in condition for allowance which is courteously solicited.

Respectfully submitted,



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Enclosures

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

Application No.: 09/582,067
Filing Date: 21 June 2000
Inventor: Erzgräber et al.

Examiner: Fordé, R.
Group Art Unit: 2826

Substitute Specification with Markings Incorporating the Preliminary Amendment of 20 June 2000 and the Amendment of 20 June 2003

Integrated Circuit with Reduced Parasitic Capacitive Influence and Method of Its Fabrication

BACKGROUND OF THE INVENTION.

1. Field of the Invention.

The invention relates to an integrated circuit with reduced parasitic capacitive influence and to a method of its fabrication.

The reduction of parasitic capacitive influence is of ever increasing significance particularly in modern CMOS technologies. If integrated circuits are being realized by bipolar technologies, substrate-inherent capacitive and ohmic losses of inductances or other passive circuit elements may be kept low by the use of high-ohmic or semi-insulating substrates. It [mus] must, however, be assumed that CMOS technologies are preferred because of lower costs, low power consumption and small dimensions.

2. The State of the Art.

The integration of passive elements, such as, for instance, inductances constitutes a pressing necessity, particularly for realizing monolithic RF transceiver switching circuits on silicon substrates. In the GHz range impedance matching for which such passive elements are necessary. If CMOS technologies satisfy the requirements for fabricating RF transceivers for cellular systems or LAN, this means, however, that because of the usually used low-ohmic Si substrates (typically 1 - 10 Ωcm) the desired high qualities of the inductances cannot be attained [a priori] *a priori*. Optimizing these

passive components, above all, is a matter of maximizing the quality factor by minimizing resistance losses and capacitive parasitics. Substrate-inherent losses may be reduced by removing the spiral path of the inductance as far as possible from the silicon substrate, for instance, by using, in a multi-layer conductor system, the uppermost layer(s) for the spiral so that, overall, a sufficiently thick insulation between spiral and substrate is yielded because of several intermediate plane insulating layers. However, since CMOS technologies measuring ≤ .5 µm utilize relatively thin insulating layers, the losses in low-ohmic silicon substrates cannot be kept sufficiently low without additional means. For reducing substrate-inherent losses such variants as the use of high-ohmic silicon wafers, the use of SOI substrates (on high-ohmic silicon wafer bases), the use of SOS substrate, removal of silicon below the spiral (air bridge), the use of dielectric materials of low relative dielectric constant, e.g., silicon dioxide as polymers, have been proposed. It has also been proposed to realize the metal spiral in a metal layer of a thickness of several µm over a very thick insulating layer, both layers being additionally formed above the CMOS structure required for the circuits. Such variants suffer from the drawback that established CMOS technologies must be modified or that the semiconductor substrates are dearer. Moreover, these variants cannot generally be used for all other passive elements of an integrated circuit, such as, in particular, resistors, capacitors, conductors and bonding pads which also are subject being influenced by parasitic capacitances.

U.S. Patent 5,548,150 discloses a field effect transistor on a SOI substrate in which for the purpose of increasing the velocity a buried insulating layer is arranged below the active layers for forming the active elements. Further applications of specific SOI substrates fabricated by wafer bonding relate to the fabrication of integrated inductances. Since the silicon is removed in the area of the spirals, undesirable differences in height will result. In alternatives, porous (and, therefore, high-ohmic) Si is used in other

embodiments for reducing parasitics.

U.S. Patent 4,910,1165 relates to a SOI process utilizing oxidized porous silicon for forming dielectric insulating epitaxial silicon islands in which active elements are subsequently realized. Here, too, an improvement in the velocity of field effect and bipolar transistor is brought about by reducing the direct capacitive coupling between the epitaxial Si island and the substrate by a thicker insulating layer.

A thick oxidized porous silicon layer on a p-silicon substrate is for planar inductances and other passive components is described by C. M. Nam et al. in "High Performance Planar Inductor on Thick Oxidized Porous Silicon Substrate", IEEE Microwave and guided wave letters, vol. 7, No. 8, pp. 236 seq. The thick insulating layer is formed as a large surface so that this substrate cannot be the starting point for a CMOS or CMOS compatible process. U.S. Patent 5,736,749 discloses an integrated circuit including an inductance. The inductance is formed above an area of porous silicon at least 200 µm thick. That corresponds to a local high-ohmic substrate area. The use of a high-ohmic substrate is one of the essential possibilities to reduce parasitic capacitances. It is not available, however, at a large wafer diameter and requires additional technological processes for latchup suppression.

OBEJCT OF THE INVENTION.

It is an object of the invention to propose an integrated circuit of reduced parasitic capacitive influences, and a method of its fabrication, in which the parasitic capacitive influences are reduced in respect of individual elements of the integrated circuit. Furthermore, the technological sequence for realizing the contact and conductor system of modern CMOS technologies is not to be adversely affected, and additional planarizing steps are not to

become necessary.

SUMMARY OF THE INVENTION.

The object is accomplished by a partial insulating layer of a thickness of at least 5 µm which is locally restricted to the area of specific passive elements of the integrated circuit and which is buried in the semiconductor substrate.

The losses arising from parasitic influences and which are dependent upon the specific electrical resistance of the silicon substrate used, are significantly reduced, so that the quality of an integrated inductance may be increased as a function of the selected thickness of the buried insulating layer by about 40 % and more, relative to planar inductances based on conventional CMOS.

The essential advantage of the insulating variant here proposed resides in the realization of the thick buried oxide realized free of stresses restricted to the area of but one subsequently formed passive element of the integrated circuit. In this manner, large differences in the structural heights and, therefore, complex planarizing measures are avoided in the subsequent technological process. Therefore, the process of fabricating strongly scaled CMOS or BiCMOS structures is not adversely affected by the necessity of inserting additional thick insulating layers between the spiral and the substrate to realize integrated inductances of high quality. The fabrication of integrated circuits in accordance with the invention is accomplished by the following steps

- masking of the surface of the silicon wafer,
- forming moats and ribs by anisotropic etching,
- an optional sacrificial oxidation, i.e. a partial anoxidation of the ribs followed by oxide removal for optimizing the ratio between the widths

of the ribs and the moats,

- total oxidation of the ribs to silicon oxide and at least filling of the moats adjacent to the surfaces by precipitating silicon dioxide,
- CMOS process or CMOS-compatible silicon process for the fabrication of the individual elements of the integrated circuit by utilization of the partial steps inherent in the given process for fabricating the elements of the integrated circuit, the passive elements of reduced parasitic influences being formed above the area of the buried thick oxide.

The advantage offered by the invention is that substrate-inherent losses of passive elements such as, for example, inductances, capacitances or resistances are significantly reduced. It is of particular advantage that all processes applied for fabricating the buried oxide area are CMOS compatible and thus do not include any unconventional method steps. Hence, established CMOS or CMOS compatible silicon technologies need not be modified, and a cost-efficient semiconductor substrate may be utilized. Especially in cases where CMOS technologies of structural dimensions of < .5 µm and very low ohmic substrates (< .1·cm) are used for latchup suppression, the use of the buried local insulation for integrated inductances is advantageous. In these substrates the Q factor and the inherent resonance frequency may be increased by at least 100 %. The solution in accordance with the invention may in general be applied to all other passive elements of an integrated circuit such as, in particular, resistances, capacitances, conductors and bonding pads which are also subject to parasitic capacitive influences.

DESCRIPTION OF THE DRAWINGS.

The characteristics of the invention are not only apparent from the claims but also from the description and the drawings, protection being sought for elements constituting patentable embodiments by themselves or

as subcombinations. Embodiments of the invention will hereinafter be explained in greater detail.

In the figures:

Fig. 1 is a schematic top elevation of the structure of an inductance;
Fig. 2 is a schematic cross-section of an inductance.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS.

Fig. 1 is a schematic top elevation depicting the structure of an inductance as part of an integrated circuit in accordance with the invention. Fig. 2 schematically depicts a cross-section of the inductance. The integrated inductance consists of an upper metal plane 1 for realizing a spiral, an insulating layer 2, a lower metal plane 3 for forming a contact of the internal connection 10, an insulating layer 4, a field oxide layer 5, a channel stop layer 6, a [buries] buried thick local insulating layer 7 as well as a semiconductor substrate 8. The field oxide layer 5 as well as the channel stop layer 6 are disposed only outside of the area of the integrated inductance. The buried thick local insulating layer 7 is arranged within the area of the inductance below the metal layers 1 and 3.

For fabricating the inductance, moats of a depth of about 10 µm, but at least a depth of 5 µm, are formed by anisotropic etching in a silicon wafer by means of an etching mask in the area of an integrated inductance to be formed in the subsequent process, i.e. alternating moats and ribs are being formed. The width of the ribs and moats is selected such that during subsequent transformation of the ribs into silicon oxide by a thermal oxidizing process the moats are closed by for a residual width of about 100 nm to 300 nm. Because of the increase in volume, ribs of a width of .8 µm and moats of a width of 1.2 µm will yield residual moats of a width of about 150 nm to 200

nm following total oxidation. Optionally, the ratio of the width of ribs and moats may be precisely realized by a preceding sacrificial oxidation or partial anoxidation of the ribs followed by removal of the oxide for reducing the width of the Si ribs and enlarging the width of the moats. The entire array of parallel moats and ribs is surrounded by a moat which is wider by about 25 %. This [moats] moat prevents prestresses, particularly at the ends of the long Si ribs during their transformation. The residual moats remaining after total oxidation are closed completely, at least near their surface, by a subsequent precipitation of silicon dioxide, for instance by a CVD process. This sequence results in a thick buried insulating layer 7 the thickness of which is defined by the depth of the etched moats. The cavities remaining in the middle area of this oxide region offer the additional advantage of an effectively reduced dielectric constant. Removal of the CVD oxide layer from the surface and of the etching mask for etching the moats is followed by the appropriate CMOS or CMOS compatible silicon process. Alternatively, the etching mask may be partially or completely removed prior to oxidation of the ribs. The integrated inductance is realized above the buried thick insulating layer 7 by using the contact and conductor system present in the CMOS process.

An integrated circuit of reduced parasitic capacitive influences and a method of its fabrication have been set forth by the present invention on the basis of a concrete example. It is to be noted, however, that the present invention is not limited to the details of the embodiments in the description as changes and mutations are being claimed within the scope of the claims. An insulating layer locally restricted to the area of the elements of the integrated circuit and buried in the semiconductor substrate is not only suitable for fabricating an integrated inductance, but also other elements of the integrated circuit, in particular further passive components such as resistors and capacitors as well as conductors and bonding pads.

[Patent Claims] What is claimed is:

1. [Integrated] An integrated circuit of reduced parasitic capacitive influences comprising an insulating layer (7) buried in the semiconductor substrate (8), characterized by the insulating layer (7) being at least 5 µm thick and is locally restricted to specific areas of the integrated circuit, i.e. to specific passive elements.

2. [Integrated] The integrated circuit according to claim 1, [characterized by the fact that] wherein the partial insulating layer (7) of a thickness of at least 5 µm is locally restricted to the area of one or more integrated inductances, one or more integrated resistors, one or more integrated capacitors, one or more integrated bonding pads and/or one or more conductors and buried in the semiconductor substrate (8).

3. [Integrated] The integrated circuit according to claim 2, [characterized by the fact that] wherein the integrated inductance consists of at least one upper metal plane (1) for realizing a spiral, [and] an insulating layer (2), a lower metal plane (3) for forming a contact of the inner connector (10), an insulating layer (4), a field oxide layer (5), a channel stop layer (6), a buried local insulating layer (7) of a thickness of at least 5 µm as well as a semiconductor substrate (8).

4. [Method] A method of fabricating an integrated circuit by means of CMOS or CMOS compatible silicon technologies with a local buried insulation, [characterized by] comprising the method steps

- masking of the surface of the silicon wafer,
- forming moats of a depth of at least 5 µm and ribs in a width ratio of about 3.2 as well as a moat wider by about 25 % drawn around the entire array of moats and ribs, by anisotropic etching,
- an optional sacrificial oxidation, i.e. a partial anoxidation of the ribs

followed by oxide removal for precisely optimizing the ratio between the widths of the ribs and the moats for the purpose of reducing prestresses and possible formation of displacement in the successive process step,

- total oxidation of the ribs to silicon oxide and at least filling of the remaining moats adjacent to the surfaces by precipitating silicon dioxide, whereby cavities remain in the middle area of the oxide area which offer the additional advantage of an effectively increased dielectric constant,
- CMOS process or CMOS-compatible silicon process for the fabrication of the individual elements of the integrated circuit by utilization of the partial steps inherent in the given process for fabricating the elements of the integrated circuit, passive elements of the integrated circuit being formed for the purpose of reduced parasitic influences directly above the area of the buried insulation layer (7) of at least 5 µm thickness.

5. [Method] The method according to claim 4, [characterized by] further comprising the process steps of

- masking of the surface of the silicon wafer,
- forming moats at least 5 Mm deep and ribs by anisotropic etching,
- an optional sacrificial oxidation, i.e. a partial anoxidation of the ribs followed by oxide removal for optimizing the ratio between the widths of the ribs and the moats,
- total oxidation of the ribs to silicon oxide and at least filling of the moats adjacent to the surfaces by precipitating silicon dioxide,
- CMOS process or CMOS-compatible silicon process for the fabrication of an inductance above the area of the buried thick oxide using the contact and conductor system present in the given process.

6. [Method] The method according to claim 4 [or 5, characterized by] further comprising the step of etching moats of a depth of at least 5 µm, the

width of the ribs and moats being selected such that during a subsequent complete transformation of the ribs into silicon dioxide by oxidation the moats are closed but for a residual width of about 100 nm to 300 nm.

7. [Method] The method according to [one or more of claims] claim 4 [to 6, characterized by the fact that] wherein moats of at least 5 µm depth are etched such that ribs of a width of about .8 µm and moats of a width of about 1.2 µm are formed and that this array of moats and ribs is surrounded by a wider moat of a width of about 1.5 µm.

8. [Method] The method according to [one or more of claims] claim 4 [to 6, characterized by the fact that] wherein the moats of a depth of at least 5 µm are etched such that ribs of a width of about .8 µm and moats of a width of about 1.2. µm are subsequently formed by an additional sacrificial oxidation step.

9. (New) An integrated circuit of reduced parasitic capacitive influences, comprising:

a semiconductor substrate; and

an insulating layer of a thickness of at least 5 µm thickness buried in the substrate and locally restricted to specific areas of the integrated circuit.

10. (New) The integrated circuit of claim 9, wherein the insulating layer is locally restricted to the area of at least one of an integrated inductance, integrated resistor, integrated capacitor, integrated bonding pad, and conductive path.

11. (New) The integrated circuit of claim 10, wherein the integrated inductance comprises at least an upper metal plane for realizing a spiral, an insulating layer, a lower metal plane for providing a connection for an internal contact, an insulation layer, a field oxide layer, a channel stop layer, the

buried local insulating layer and the semiconductor substrate.

12. (New) An integrated circuit of reduced parasitic capacitive influences, comprising:

a semiconductor substrate; and

an insulating layer of a thickness of at least 5 μm thickness buried in the substrate and locally restricted to the area of at least one of an integrated inductance, integrated resistor, integrated capacitor, integrated bonding pad and conductive path, wherein the integrated inductance comprises at least an upper metal plane for realizing a spiral, an insulating layer, a lower metal plane for providing a connection for an internal contact, an insulation layer, a field oxide layer, a channel stop layer, the buried local insulating layer and the semiconductor substrate.

[Abstract] ABSTRACT OF THE DISCLOSURE

The invention relates to an integrated circuit of reduced parasitic capacitive influences and to a method of its fabrication. It is an object of the invention to propose an integrated circuit of reduced parasitic capacitive influences and a method of its fabrication in which the parasitic capacitive influences for individual especially passive elements of the integrated circuit is reduced. In addition, the technological sequence for realizing the contact and conductor system of modern CMOS or CMOS compatible silicon technologies is not to be adversely affected during the fabrication of circuits with integrated passive elements and, in particular, no additional planarizing steps are to become necessary. The object is accomplished by an at least partial insulating layer of a thickness of at least 5 μm which is locally restricted to the area of the elements of the integrated circuit and which is buried in the semiconductor substrate. The losses caused by parasitic influences and dependent upon the specific electrical resistance of the silicon substrate used, are significantly reduced so that depending upon the selected thickness of the buried insulating layer, the quality of an integrated inductance may be improved by about 40 % or more relative to planar inductances based upon conventional CMOS.